PRG

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/161,405	09/28/1998	HIRAKU KOZUKA	862.2480	7603

5514 7590 09/11/2002

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WHIPKEY, JASON T	
ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/161,405	KOZUKA, HIRAKU	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 28* is/are rejected.

7)☒ Claim(s) *27 and 29-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3,6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1A, 1B, and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference signs not mentioned in the description: ΦBB, ΦN1, ΦCR, V_{CHR}, 99, ΦERS, and ΦTT. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference signs in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "13" has been used to designate both an amplifier (Figure 1A) and an analog switch (Figure 4A). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

6. The disclosure is objected to because of the following informalities:

- Line 20 of page 11 ends the series of sensor chips with "100_n", where "100^n" would be the correct notation.
- Line 14 of page 15 indicates that analog switch 15 is in Figure 4A, but that part is not located in that figure.

Appropriate correction is required.

Claim Objections

7. Claim 1 is objected to because of an informality. Line 10 indicates "a common output lines." Appropriate correction is required. For examination purposes, the examiner will interpret the claim to read "a common output line."

8. Claim 26 is objected to as failing to comply with 37 CFR 1.75(a) for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 26 recites the limitation "the designated photosensor chip" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the examiner will interpret that claim to read "a single designated photosensor chip."

Claim 26 recites the limitation "the changed photosensor chip" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the examiner will interpret that claim to read "the other photosensor chip."

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 1-4 are rejected under 35 U.S.C. 101 because the claims are directed to neither a process nor a machine. Each of the claims recites *both* an image sensor and a method of driving the same. Therefore, it does not fall into *one* of the statutory classes set forth by 35 U.S.C. 101. See MPEP §2173.05(q).

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-4 and 6-7, 9-10, 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. Claims 1-4 each recite both an image sensor and a method of driving the same. Consequently, these claims are indefinite under 35 U.S.C. 112, second paragraph. See MPEP §2173.05(q).

14. Claim 2 recites the limitations "noise and light signal common output line" (lines 22 and 26) and "said common output line" (line 41). There is insufficient antecedent basis for this limitation in the claim. Lines 15-18 indicate that the image sensor has a noise signal common output line and a light signal common output line. For examination purposes, the examiner will interpret the claim such that the reset means resets both lines and capacitance division is performed on both lines.

15. Claim 3 recites the limitation "common output line" on lines 22 and 41. There is insufficient antecedent basis for this limitation in the claim. Lines 12-15 indicate that the image sensor has a noise signal common output line and a light signal common output

line. For examination purposes, the examiner will interpret the claim such that the reset means resets both lines.

16. Claim 6 recites the limitation "noise and light signal common output line" on lines 20-21 and 24-25. There is insufficient antecedent basis for this limitation in the claim. Lines 14-17 indicate that the image sensor has a noise signal common output line and a light signal common output line. For examination purposes, the examiner will interpret the claim such that the reset means resets both lines and capacitance division is performed on both lines.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 22-24, 26, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura.

Regarding claims 22 and 32, Nakamura teaches an image sensor consisting of multiple sensor chips, each with a number of photoconversion cells (column 2, lines 66-68). Each chip — 1-1 in Figure 1, for example — has a bus (unlabeled) connecting the

drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. Shift registers 8-1-1, 8-1-2, etc. and transistors 6-1-1, 6-1-2, etc. act as a fan-out circuit by selecting an individual photoconversion cell for output onto the bus (column 3, lines 43-50).

The sensor chips are connected with a common output bus, ending with terminal 23. An amplifier circuit, consisting of parts 33-39 shown in Figure 3, receives the output of the inter-chip bus. Buffer amplifier 33 receives the signals from the bus and sends them to the clamping circuit consisting of parts 35-38. The clamping circuit clamps the output of buffer amplifier 33 using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12). The switch is then turned off so the line is floating (column 4, lines 13-16). Buffer amplifier 39 then receives the clamped output and outputs the signal to signal processor 40. The clamping corrects the variation of offsets between the chips (column 4, lines 54-57). This occurs for each chip before the light signals are read out (column 4, lines 2-7).

Regarding claim 23, the chips are aligned (column 3, lines 2-4), indicating they are mounted on a base one dimensionally.

Regarding claim 24, components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

Regarding claim 26, shift registers 8-1-1, 8-1-2, etc. perform all timing functions for the chips. A pulse placed on voltage terminal 25 selects chip 1-1 and outputs the signal of each photoconversion cell one at a time onto the intra-chip bus, as described

above (column 3, lines 43-55). Control signal source 36 enables and disables the clamping circuit (column 4, lines 13-16).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. All of the rejections below over Nakamura refer to U.S. Patent No. 5,321,528.

21. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki.

Regarding claim 1, Nakamura teaches an image sensor consisting of multiple sensor chips that are aligned (column 2, line 66, through column 3, line 4), indicating they are mounted on a base one dimensionally. Each chip — 1-1 in Figure 1, for example — has an output bus (unlabeled) connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. Signals representative of light are held in capacitors 7-1-1 to 7-n-m (column 3, lines 21-23). The output bus in each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). The line is reset via reset terminal

24 (column 3, lines 39-40). Amplifiers 9-1 *et al.* output the signal from the output bus of each chip.

An amplifier circuit, consisting of parts 33-39 shown in Figure 3, receives the output of an inter-chip bus. Buffer amplifier 33 receives the both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12). Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Nakamura is silent with regard to using signal holding means to hold noise signals from the photoconversion cells.

Miyazaki discloses an image pickup device (Figure 4) that has a capacitor 3A for each cell that holds a light signal and a capacitor 3B that holds a noise signal (column 4, line 62, through column 5, line 8). An advantage to using a separate capacitor for a noise signal is that the capacitor may be read out while the cell is integrating a light signal, which allows the sensor to implement longer integration times. For this reason, it would have been obvious to have Nakamura's sensor system provided with a noise capacitor for each cell.

Claim 5 may be treated like claim 1. However, Nakamura is silent with regard to including the sensor module on the substrate with the processing means. The advantage to doing so is that the sensor module and the processing means may be connected using the printed circuits, which eliminates the need for wiring between the two parts. For this reason, it would have been obvious to have Nakamura include the sensor module and processing means on the same substrate.

22. Claims 2-4, 6, 7, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Shinohara.

Regarding claims 2, 3, and 6, Nakamura teaches an image sensor consisting of multiple sensor chips that are aligned (column 2, line 66, through column 3, line 4), indicating they are mounted on a base one dimensionally. Each chip — 1-1 in Figure 1, for example — has an output bus (unlabeled) connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. Signals representative of light are held in capacitors 7-1-1 to 7-n-m (column 3, lines 21-23). The output bus in each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). The line is reset via reset terminal 24 (column 3, lines 39-40). Amplifiers 9-1 *et al.* output the signal from the output bus of each chip.

Buffer amplifier 33 receives the both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Capacitor 35 is part of a

clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12). Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Nakamura is silent with regard to using signal holding means to hold noise signals from the photoconversion cells and using separate noise and light signal output lines.

Miyazaki discloses an image pickup device (Figure 4) that has a capacitor 3A for each cell that holds a light signal and a capacitor 3B that holds a noise signal (column 4, line 62, through column 5, line 8). The light and noise signals are output onto lines 7A and 7B, respectively. These lines may be reset by transistors 9A and 9B (column 5, lines 26-29).

An advantage to using a separate capacitor for a noise signal is that the capacitor may be read out while the cell is integrating a light signal, which allows the sensor to implement longer integration times. For this reason, it would have been obvious to have Nakamura's sensor system provided with a noise capacitor for each cell.

An advantage to using separate noise and light output lines is that less switching is necessary in each pixel, which reduces the size of each pixel. For this reason, it

would have been obvious to have Nakamura's sensor system provided with separate light and noise output lines.

Both Nakamura and Miyazaki are silent with regard to the output lines being read using capacitance division.

Shinohara discloses an image sensor with one of the capacitors 7 connected to output line 9 when a column is selected (Figure 1). The capacitance of capacitors 7 is chosen so that capacitance division may be used advantageously (column 9, lines 17-19). As stated in column 9, lines 24-28, capacitance division decreases readout destruction and increases the S/N ratio of the outputted signal. For this reason, it would have been obvious for Nakamura to utilize capacitance division on the output lines.

Claim 7 may be treated like claim 6. However, Nakamura is silent with regard to including the sensor module on the substrate with the processing means. The advantage to doing so is that the sensor module and the processing means may be connected using the printed circuits, which eliminates the need for wiring between the two parts. For this reason, it would have been obvious to have Nakamura include the sensor module and processing means on the same substrate.

Regarding claims 4 and 15, Nakamura teaches an image sensor consisting of multiple sensor chips that are aligned (column 2, line 66, through column 3, line 4), indicating they are mounted on a base. Each chip — 1-1 in Figure 1, for example — has an output bus (unlabeled) connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. Signals representative of light are held in capacitors 7-1-1 to 7-n-m (column 3, lines 21-23). The output bus in

each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). The line is reset via reset terminal 24 (column 3, lines 39-40). Amplifiers 9-1 *et al.* output the signal from the output bus of each chip.

An amplifier circuit, consisting of parts 33-39 shown in Figure 3, receives the output of an inter-chip bus. Buffer amplifier 33 receives the both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Buffer amplifier 33 acts as a signal input buffer means and a gain amplifier. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12). Buffer amplifier 39 receives the clamped signal. Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Nakamura is silent with regard to using signal holding means to hold noise signals from the photoconversion cells.

Miyazaki discloses an image pickup device (Figure 4) that has a capacitor 3A for each cell that holds a light signal and a capacitor 3B that holds a noise signal (column 4, line 62, through column 5, line 8). An advantage to using a separate capacitor for a noise signal is that the capacitor may be read out while the cell is integrating a light

signal, which allows the sensor to implement longer integration times. For this reason, it would have been obvious to have Nakamura's sensor system provided with a noise capacitor for each cell.

Both Nakamura and Miyazaki are silent with regard to the output lines being read using capacitance division.

Shinohara discloses an image sensor with one of the capacitors 7 connected to output line 9 when a column is selected (Figure 1). The capacitance of capacitors 7 is chosen so that capacitance division may be used advantageously (column 9, lines 17-19). As stated in column 9, lines 24-28, capacitance division decreases readout destruction and increases the S/N ratio of the outputted signal. For this reason, it would have been obvious for Nakamura to utilize capacitance division on the output lines.

Claim 16 may be treated like claim 15. However, Nakamura is silent with regard to including the sensor module on the substrate with the processing means. The advantage to doing so is that the sensor module and the processing means may be connected using the printed circuits, which eliminates the need for wiring between the two parts. For this reason, it would have been obvious to have Nakamura include the sensor module and processing means on the same substrate.

23. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Surisawa.

Claim 8 may be treated like claim 5. However, both Nakamura and Miyazaki are silent with regard to using a power supply voltage with the photosensor chips that is lower than the power supply voltage supplied to the processing means.

Surisawa discloses an image sensor on a substrate 1 (Figure 10A). The voltage V_{sub} supplied to the substrate is larger than the voltage V_D supplied to the image sensor (column 13, lines 6-8). The advantage to having separate power supplies is that the appropriate voltage may be supplied to each component without excess, which saves power. For this reason, it would have been obvious to have separate power supplies for the chips and the substrate.

24. Claims 9, 10, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Shinohara and Surisawa.

Claims 9, 10, 17, and 18 may be treated like claims 6, 7, 15, and 16, respectively. However, Nakamura, Miyazaki, and Shinohara are all silent with regard to using a power supply voltage with the photosensor chips that is lower than the power supply voltage supplied to the processing means.

Surisawa discloses an image sensor on a substrate 1 (Figure 10A). The voltage V_{sub} supplied to the substrate is larger than the voltage V_D supplied to the image sensor (column 13, lines 6-8). The advantage to having separate power supplies is that the appropriate voltage may be supplied to each component without excess, which saves

power. For this reason, it would have been obvious to have separate power supplies for the chips and the substrate.

25. Claims 12, 13, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Shinohara and Hamasaki.

Claims 12, 13, 19, and 20 may be treated like claims 6, 7, 15, and 16, respectively. However, Nakamura, Miyazaki, and Shinohara are all silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

26. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Hamasaki.

Claim 11 may be treated like claim 5. However, Nakamura and Miyazaki are both silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Surisawa and Hamasaki.

Claim 14 may be treated like claim 8. However, Nakamura, Miyazaki, and Surisawa are all silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

28. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Shinohara, Surisawa and Hamasaki.

Claim 21 may be treated like claim 17. However, Nakamura, Miyazaki, Shinohara, and Surisawa are all silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

29. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura.

Claim 25 may be treated like claim 22. However, Nakamura is silent with regard to including the sensor module on the same board with the amplifier and processing means. The advantage to doing so is that the sensor module and the processing means may be connected using the printed circuits, which eliminates the need for wiring between the two parts. For this reason, it would have been obvious to have Nakamura include the sensor module and processing means on the same substrate.

30. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Miyazaki and further in view of Hatanaka.

Claim 28 may be treated like claim 22. Additionally, Nakamura teaches that capacitor 35 receives the light and noise signals from each of the chips and finds the difference (column 4, lines 16-30).

However, Nakamura is silent with regard to having the inter-chip bus utilize separate light and dark signal lines and using a differential amplifier.

Miyazaki discloses an image pickup device. Light and noise signals generated in each pixel are output onto lines 7A and 7B, respectively, as shown in Figure 4. These signals are fed to a differential amplifier 21.

An advantage to using separate noise and light output lines is that less switching is necessary in each pixel, which reduces the size of each pixel. For this reason, it would have been obvious to have Nakamura's sensor system provided with separate light and noise output lines.

An advantage to using a differential amplifier is that it combines difference-calculating circuitry with an amplifier, thereby reducing the number of components in the system. For this reason, it would have been obvious to have Nakamura's system include a differential amplifier.

Miyazaki is silent with regard to having a source-follower circuit connected to the light and dark signal lines.

Hatanaka discloses a photoelectric conversion apparatus, as shown in Figure 2. The system includes a switch array 11, shown in detail in Figure 3. Common signal lines 102 and 103 are connected source-follower FETS 110 and 111, respectively (column 3, lines 60-62). As stated in column 4, lines 28-33, the source-follower transistors 110 and 111 act as buffers, allowing a large number of pixels to be connected to the differential amplifier. For this reason, it would have been obvious to have Miyazaki's system include a source follower on each output line.

Allowable Subject Matter

31. Claims 27 and 29-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 27, no prior art could be located that teaches or fairly suggests a gain circuit juxtaposed between two clamping circuits, wherein the second clamping circuit clamps the output signal each time a new image sensor is selected.

Regarding claim 29, no prior art could be located that teaches or fairly suggests a clamping circuit that begins and ends clamping before light and dark current signals are captured by a photosensor chips.

Claims 30 and 31 are objected to as being dependent on claim 29.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 8 A.M. to 5:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned are (703) 872-9314 for both regular communication and After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to (703) 872-9314 for either formal or informal communications intended for entry. (For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**.)

Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW

JTW
September 5, 2002

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600